REMARKS

Reconsideration of this application, in view of the foregoing amendments and the following remarks, is respectfully requested.

Claim Rejections - 35 USC § 102

 Claims 1-3 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiguchi et al. (USP 5275393). Applicants respectfully traverse these rejections.

To anticipate a claim, the reference must teach each and every limitation of the claim. M.P.E.P. §2131. As to claim 1, Horiguchi et al. does not teach each and every limitation of the claim.

Applicants would like to point to the Examiner that there is a very basic and fundamental difference between what is recited in claims 1 and 2 and cited by the Examiner. Claim 1 recites a primary current block generating a primary bias current using a second supply voltage, wherein said second supply voltage is less than said first supply voltage. In a complete contrast, Horiguchi et al. teaches using the larger of the two voltages (please see col. 7, lines 19-28, figures 2a-b). Further as to claim 2, the Examiner has stated that "figure 10 shows that the multiplexor selects the backup bias current as the bias current when the second supply voltage is not present (when V2 is lower than V1)." (Emphasis added). In fact, Horiguchi et al. teaches completely opposite of what the Examiner has stated. According to Horiguchi, et al. as long as the external supply voltage Vcc (V) stays within 5+/- 0.5 volts, V1 = V1 and when the Vcc reaches 6 volts, V1 = V2. Thus, "a higher voltage than in ordinary operation is impressed on the internal voltage, so that the voltage aging of the internal circuit be conducted." (col. 7, lines 29-56, figure 2b). Accordingly, Horiguchi et al. teach completely opposite of what is recited in claims 1-2 and therefore, does not anticipate claims 1-2.

As to claim 3, the Examiner has stated that "As to claim 3, figure 2 shows that the multiplexor performs the selecting according to a select signal (output of 4) connected to a node..." (emphasis added). Applicants respectfully point to the Examiner that actually, the

switch 3 receives a control signal from comparator 4 and it is not connected to a node. The switch 3 independently connects to either V1 or V2 (see figure 2a). Accordingly, Horiguchi does not teach this limitation.

Claim Rejections -35 USC §103

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horiguchi et al. (USP 5275393) in view of Yamauchi (USP 5982162) (previously cited). Applicants respectfully traverse this rejection.

Claim 4 depends from claim 1 and is patentably distinguishable from the cited reference for at least the same reasons as claim 1.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horiguchi et al. (USP 5275393) in view of Yamauchi (USP 5982162) and Wang (USP 5939933).

Claim 5 depends from claim 1 and is patentably distinguishable from the cited reference for at least the same reasons as claim 1.

Applicant believes this application and the claims herein to be in a condition for allowance. Please charge any additional fees, or credit overpayment to Deposit Account No. 20-0668. Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,

/Abdul Zindani/

Abdul Zindani Attorney for Applicant Reg. No. 46,091

Texas Instruments Incorporated P.O. Box 655474, MS 3999 Dallas, TX 75265 (972) 917-5137